DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 50-51 are rejected under 35 U.S.C. 102(e) as being anticipated by Kubota et al. [U.S. Pat. 7,094,639] previously applied.

With respect to claim 50, Kubota et al. (fig. 1, cols. 5-6) disclose a semiconductor device comprising a MIS type field effect transistor, wherein the transistor comprises:

a silicon substrate (11),

a gate insulating film comprising a high-dielectric-constant metal oxide film (14) and a silicon containing insulating film (13) lying between the metal oxide film and the silicon substrate; and

a silicon containing gate electrode (15) formed on the gate insulating film, a gate length of said silicon containing gate electrode being not greater than 1 μm (col. 1, lines 18-20).

With respect to claim 51, Kubota et al. (fig. 1, col. 6 lines 2-4) disclose that the transistor further comprises a silicon nitride film (18) formed so as to cover a lateral face of the high-dielectric-constant metal oxide film.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1-2, 9-12, 25-27, 48-49 and 52-53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu et al. [U.S. Pat. 6,913,980] previously applied, in view of Kubota et al. [U.S. Pat. 7,094,639] previously applied.

With respect to claims 1 and 48-49, Wu et al. (fig. 23, cols. 5-11) disclose a semiconductor device comprising a MIS type field effect transistor, wherein the transistor comprising:

a silicon substrate (304);

a gate insulating film (312) comprising a high-dielectric-constant metal oxide film and a silicon containing insulating film (col. 6, lines 9-23 and col. 8, lines 25-27) formed on the silicon substrate;

a silicon containing gate electrode (310) formed on the gate insulating film; and

a sidewall (336) including silicon oxide as a constituting material, which is formed on each lateral face side of the gate electrode; and

wherein a silicon nitride film (330) is interposed between the sidewall and at least the lateral face of the gate electrode, and wherein the silicon nitride film covers the lateral face of the high-dielectric-constant metal oxide film, and a silicon oxide film (328) underlies the silicon nitride film.

Wu et al. fail to disclose a silicon containing insulating film lying between the metal oxide film and the silicon substrate and a gate length of the silicon containing gate electrode being not greater than 1 μm (200 nm, 100 nm in claims 48-49, respectively). However, Kubota et al. disclose that the silicon containing insulating film (13) lying between the metal oxide film (14) and the silicon substrate (11) (fig. 1 and col. 5, lines 47-49) and a gate length of the silicon containing gate electrode being not greater than 0.1 μm (100 nm) (col. 1, lines 18-20). Therefore, it would have been obvious to one having skill in the art to use the silicon containing insulating film lying between the metal

oxide film and the silicon substrate as taught by Kubota et al. into the device of Wu et al. in order to prevent a reaction between the silicon substrate and the high dielectric constant. It is noted that, the gate length range would have been obvious to an ordinary artisan practicing the invention because, absent evidence of disclosure of criticality for the range giving unexpected results, it is not inventive to discover optimal or workable ranges by routine experimentation. *In re Aller*, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). Furthermore, it appears that these changes produce no functional differences and therefore would have been obvious. See *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990). Therefore, it would have been obvious to one having skill in the art to combine the feature of Kubota with the device disclosed in Wu to reduce the scale of the MISFET device.

With respect to claim 2, Wu et al. (fig. 23) disclose that the silicon nitride film (330) is laid between the sidewall and the silicon substrate.

With respect to claim 9, Kubota et al. (fig. 1 and col. 6, lines 36-39) disclose that a silicon nitride film (13) is laid between the high-dielectric-constant metal oxide film and the gate electrode.

With respect to claims 10-11, Wu et al. (fig. 23 and col. 6, lines 17-18) disclose that the high-dielectric-constant metal oxide film contains hafnium (Hf) and a dielectric

constant of the high-dielectric-constant metal oxide film (Hf) is not less than 10.

With respect to claim 12, Wu et al. (fig. 23 and col. 6, lines 36-39) disclose that the high-dielectric-constant metal oxide film is absent beneath the sidewall.

With respect to claim 25, Wu et al. (fig. 23 and col. 9, lines 31-32) disclose that a thickness of the silicon oxide film is within a range of 1 to 20 nm.

With respect to claims 26-27 and 52-53, Wu et al. does not teach the exact thickness range of the silicon oxide film and the silicon nitride film, as claimed by Applicant. However, the thickness range would have been obvious to an ordinary artisan practicing the invention because, absent evidence of disclosure of criticality for the range giving unexpected results, it is not inventive to discover optimal or workable ranges by routine experimentation. *In re Aller*, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). Furthermore, it appears that these changes produce no functional differences and therefore would have been obvious. See *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Response to Arguments

6. Applicant's arguments filed August 20, 2007 have been fully considered but they are not persuasive.

Applicant argues that Kobuta would not have been combined with Wu as alleged by the Examiner wherein the primary reference Wu is not taught or suggested " a gate length of said silicon containing gate electrode being not greater than 1μm. The Examiner has failed to establish a *prima facie* case of obviousness and the Examiner

has not provided any reason why one of ordinary skill in the art would have combined this alleged feature of Kubota with the device disclosed in Wu.

Applicant's argument are not persuasive because with recent technological advance with respect to high integration and high speed in semiconductor devices, miniaturization of MISFETs has been under development and the smaller gate length of the MISFET is required. Kobuta discloses a gate length of said silicon containing gate electrode being not greater than 0.1μm (col. 1, lines 18-20). Therefore, it would have been obvious to one of ordinary skill in the art to combine the feature of Kubota with the device disclosed in Wu to reduce the scale of the MISFET device.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

8. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoai v. Pham whose telephone number is 571-272-1715. The examiner can normally be reached on M-F.

10. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

11. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Hoai v Pham/
Primary Examiner, Art Unit 2814